IN THE CLAIMS:

1. (Currently Amended) Active current mode sampling circuit comprising:

[[-]] an operational amplifier (103);

[[-]] at least one switched capacitor (C2, C2a, C2b);

[[-]] first switching elements (S101a, S102a; SlOlb, S102b) for switching said at least one switched capacitor (C2, C2a, C2b) between an input and an output of said operational amplifier (103) during charging phases (ϕ1) and for disconnecting said at least one switched capacitor (C2, C2a, C2b) from said input and said output of said operational amplifier (103) in between said charging phases (ϕ1) ; and

[[-]] second switching elements (S103a, S104a; S103b, S104b) for connecting said at least one switched capacitor (C2, C2a, C2b) during discharging phases (ϕ2) in between said charging phases (ϕ1) to a subsequent stage (104), in order to provide a charge of said at least one switched capacitor (C2, C2a, C2b) to said subsequent stage (104), and for disconnecting said at least one switched capacitor (C2, C2a, C2b) from said subsequent stage (104), respectively, in between said discharging phases (ϕ2).

2. (Original) Active current mode sampling circuit according to claim 1, wherein said at least one switched capacitor (C2, C2a, C2b) includes a first switched capacitor (C2a) which is switched by said switching elements (SlOla, S102a; S101b, S102b) between a first input and a first output of said operational amplifier (103) during said charging phases (ϕ1), and a second switched capacitor (C2b) which is switched by said switching elements (S101a, S102a ; S101b, S102b) between a second input and a second output of said operational amplifier (103) during said charging phases (ϕ1).

3. (Currently Amended) Active current mode sampling circuit according to claim 1 ~~or 2~~, further comprising at least one continuous time capacitor (Cl, Cla, Clb), which at least one continuous time capacitor (Cl, Cla, Clb) is connected fixedly to an input and an output of said operational amplifier (103).

4. (Currently Amended) Active current mode sampling circuit according to claim 3, further comprising

[[-]] at least one pair of a further switched capacitor (C2.1, C2.2) and a further continuous time capacitor (Cl. 1, C1. 2), both arranged in parallel to said at least one switched capacitor (C2) and to said at least one continuous time capacitor (Cl) ; and

[[-]] switching elements (S121. 1, 122. 1,121. 2,122. 2) for connecting a continuous time capacitor (Cl. 1, C1. 2) of selected pairs of a further switched capacitor (C2.1,

C2.2) and a further continuous time capacitor (Cl. 1, Cl. 2) continuously between said input and said output of said operational amplifier (103);
[[-]] switching elements (S123. 1, S124. 1, S123. 2, S124. 2) for switching a switched capacitor (C2. 1, C2.2) of said selected pairs of a further switched capacitor (C2.1, C2.2) and a further continuous time capacitor (Cl. 1, C1. 2) between said input and said output of said operational amplifier (103) during said charging phases (ϕ1) and for disconnecting said at least one switched capacitor (C2) from said input and said output of said operational amplifier (103) in between said charging phases (ϕ1) ; and
[[-]] switching elements (S125. 1, S126. 1, S125. 2, S126. 2) for switching a switched capacitor (C2.1, C2.2) of said selected pairs of a further switched- capacitor (C2.1, C2.2) and a further continuous time capacitor (Cl. 1, C1. 2) on both sides to ground during said discharging phases (ϕ2).

5. (Original) Active current mode sampling circuit according to claim 4, further comprising a gain control portion (111) for selecting said pairs of a further switched capacitor (C2.1, C2.2) and a further continuous time capacitor (Cl. 1, C1. 2) in accordance with a required gain.

6. (Currently Amended) Active current mode sampling circuit according to ~~one of claims 1 to 3~~claim 1, wherein said at least one switched capacitor (C2a, C2b) is divided into a plurality of switched capacitor units (C2. 1, C2.2) connected in parallel to each other, said second switching elements (S134. 1,135. 1,134. 2,135. 2) being controlled for connecting selected ones of said switched capacitor units (C2. 1, C2.2) to said subsequent stage (104) during said discharging phases (ϕ2).

7. (Original) Active current mode sampling circuit according to claim 6, further comprising a gain control portion (111) for selecting said switched capacitor units (C2.1, C2.2) in accordance with a required gain.

8. (Currently Amended) Active current mode sampling circuit according to ~~one of the preceding claims~~claim 1, further comprising a transconductance portion for converting a received voltage mode signal into a current mode signal and for providing said current mode signal to an input of said operational amplifier.

9. (Currently Amended) Active current mode sampling circuit according to ~~one of claims 1 to 7~~claim 1, further comprising

[[-]] a transconductance portion (100) for converting a received voltage mode signal into a current mode signal; and
[[-]] a frequency down-conversion portion (101) for frequency down-converting a current mode signal output by said transconductance portion and for providing said frequency down-converted current mode signal to an input of said operational amplifier (103).

10. (Currently Amended) Device (107) comprising an active current mode sampling circuit according to ~~one of the preceding claims~~claim 1.

11. (Currently Amended) Method of operating an active current mode sampling circuit, which active current mode sampling circuit includes an operational amplifier (103) and at least one switched capacitor (C2, C2a, C2b), said method comprising:
[[-]] switching said at least one switched capacitor (C2, C2a, C2b) between an input and an output of said operational amplifier (103) during charging phases (ϕ1);
[[-]] disconnecting said at least one switched capacitor (C2, C2a, C2b) from said input and said output of said operational amplifier (103) in between said charging phases (ϕ1) ;
[[-]] connecting said at least one switched capacitor (C2, C2a, C2b) during discharging phases (ϕ2) in between said charging phases (ϕ1) to a subsequent stage (104), in order to provide a charge of said at least one switched capacitor (C2, C2a, C2b) to said subsequent stage (104); and
[[-]] disconnecting said at least one switched capacitor (C2, C2a, C2b) from said subsequent stage (104) in between said discharging phases (ϕ2).

12. (Original) Method according to claim 11, wherein said at least one switched capacitor (C2, C2a, C2b) includes a first switched capacitor (C2a) and a second switched capacitor (C2b), said method comprising switching said first switched capacitor (C2a) between a first input and a first output of said operational amplifier (103) during said charging phases (ϕ1), and switching said second switched capacitor (C2b) between a second input and a second output of said operational amplifier (103) during said charging phases (ϕ1).

13. (Currently Amended) Method according to claim 11 ~~or 12~~, wherein said active current mode sampling circuit further includes at least one continuous time capacitor (Cl) which is connected fixedly to an input and an output of said

operational amplifier (103), and at least one pair of a further switched capacitor (C2.1, C2.2) and a further continuous time capacitor (Cl. 1, C1. 2), both arranged in parallel to said at least one switched capacitor (C2) and to said at least one continuous time capacitor (C1), said method further comprising

[[-]] connecting a continuous time capacitor (Cl. 1, C1. 2) of selected pairs of a further switched capacitor (C2. 1, C2.2) and a further continuous time capacitor (Cl. 1, C1. 2) continuously between said input and said output of said operational amplifier (103);

[[-]] switching a switched capacitor (C2.1, C2.2) of said selected pairs of a further switched capacitor (C2. 1, C2.2) and a further continuous time capacitor (Cl. 1, C1. 2) between said input and said output of said operational amplifier (103) during said charging phases (ϕ1), and disconnecting said at least one switched capacitor (C2) from said input and said output of said operational amplifier (103) in between said charging phases (ϕ1) ; and

[[-]] switching a switched capacitor (C2.1, C2.2) of said selected pairs of a further switched capacitor (C2. 1, C2.2) and a further continuous time capacitor (Cl. 1, C1. 2) on both sides to ground during said discharging phases (ϕ2).

14. (Original) Method according to claim 13, further comprising selecting said pairs of a further switched capacitor (C2.1, C2.2) and a further continuous time capacitor (Cl. 1, C1. 2) in accordance with a required gain.

15. (Currently Amended) Method according to claim 11 ~~or 12~~, wherein said at least one switched capacitor (C2a, C2b) is divided into a plurality of switched capacitor units (C2.1, C2.2) connected in parallel to each other, said connecting of said at least one switched capacitor (C2a, C2b) to a subsequent stage (104) during said discharging phases (ϕ2) comprising connecting selected ones of said switched capacitor units (C2.1, C2.2) to a subsequent stage (104) during said discharging phases (ϕ2).

16. (Original) Method according to claim 15, further comprising selecting said switched capacitor units (C2.1, C2.2) in accordance with a required gain.

17. (Currently Amended) Method according to ~~one of~~ claim 11 ~~to 16~~, further comprising converting a received voltage mode signal into a current mode signal and providing said current mode signal to an input of said operational amplifier.

18. (Currently Amended) Method according to ~~one of~~ claim 11 ~~to 16~~, further comprising converting a received voltage mode signal into a current mode signal, frequency down-converting said current mode signal and providing said frequency down-converted current mode signal to an input of said operational amplifier (103).